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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,164	HIROSE, YUKITOSHI	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 39-43* is/are pending in the application.

4a) Of the above claim(s) *39-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *39-43* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 16, 2008 has been entered.

Response to Amendment

This Office action is in response to Applicant's communication filed June 16, 2008 in response to the Office action dated February 15, 2008. Claims 1, 2, and 5 have been amended. New claims 39-43 have been added. Claims 1-20 and 39-43 are pending in this application.

Election/Restrictions

1. Newly submitted claims 39-43 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 1-20 and claims 39-43 are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, claims 1-20 have a separate

utility such as allowing a ring bus to continue operation when one of a plurality of memory modules is replaced while claims 39-43 have a separate utility such as allowing certain ports/terminals in a memory module to send and/or receive data.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 39-43 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

OBJECTIONS

Claims

2. In view of Applicant's amendment, the objection to **claim 1** is withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonella et al. (U.S. Patent 6,658,509) (hereinafter "Bonella") in view of Arimilli et al. (U.S. Patent Application Publication 2002/0078280) (hereinafter

"Arimilli") and Chow et al. (U.S. Patent Application Publication 2002/0069317) (hereinafter "Chow").

5. **As per claim 1**, Bonella discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data (Fig. 3; col. 8, lines 41-46; Figs. 13A and 13B, elements 140A-140H and 142A-142H) and buffer sections for sending and receiving the data (col. 9, line 40 – col. 10, line 7; Fig. 15);

a CPU which controls said control device for access operation to said memory modules (col. 1, lines 23-28), *It should be noted that the "memory controller" is analogous to the "control device."*

wherein said buffer sections are connected in series to form a ring bus with said control device (col. 3, lines 48-50; Fig. 3);

Bonella does not disclose a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a control device which, when an arbitrary memory module is being replaced, switches an operational mode of a ring bus from a unidirectional bus which either send or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally, detects an address space of said memory module to be replaced, and accesses a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module being replaced is requested;

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Arimilli discloses a control device which, when an arbitrary memory module is being replaced, switches an operational mode of a ring bus from a unidirectional bus which either send or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally (paragraph 0016; paragraph 0019; paragraph 0005; paragraph 0014; Fig. 1; Fig. 2); *When taking into account that mode selection can be accomplished by detecting "environmental characteristics" of transmission lines TL1 and TL2 combined with the fact module 12 is hot-pluggable, it follows that Arimilli allows for mode selection to be based on the hot insertion/removal of module 12 because such hot insertion/removal would change the "environmental characteristics" of transmission lines TL1 and TL2.*

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus (paragraph 0017; Fig. 2, element 22);

a second buffer circuit for sending a signal to one input/output end of the ring bus (paragraph 0017; Fig. 2, element 21);

a third buffer circuit for receiving a signal from the other input/output end of the ring bus (paragraph 0018; Fig. 2, element 24);

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus (paragraph 0018; Fig. 2, element 25);

Bonella and Arimilli are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Arimilli's mode selectable transmitter/receiver within Bonella's memory controller such that when an arbitrary memory module is being replaced, the memory controller switches an operational mode of a ring bus from a unidirectional bus which either send or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of the increased flexibility provided by a memory module system that is selectable between a bidirectional mode and a unidirectional mode.

The combination of Bonella/Arimilli does not disclose a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a control device which detects an address space of said memory module to be replaced, and accesses a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module being replaced is requested.

Chow discloses a hard disk device to which the data stored in said memory modules is copied at predetermined time periods (paragraphs 0135-0136; paragraph 154; Fig. 14, elements 110, 130, and 425); *It should noted that "non-volatile storage module" includes hard drive disks and is therefore analogous to "hard disk device" and "memory matrix module" is analogous to "memory module."*

a control device which detects an address space of said memory module to be replaced, and accesses a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module being replaced is requested (paragraph 0168; Fig. 14, element 125). *It should be noted that "management module" is analogous to "control device." It should also be noted that in order for the failover process to be completely transparent to the data processing system it is required the management module detect a memory space in the failed memory matrix module and subsequently access a memory area in the non-volatile storage module corresponding to the detected address space when an access to the memory matrix module that failed is requested.*

The combination of Bonella/Arimilli and Chow are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chow's non-volatile storage module and management module within Bonella/Arimilli's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of a storage system that is scalable, fault-tolerant, and easily maintained.

6. **As per claim 3**, the combination of Bonella/Arimilli/Chow discloses a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module (Bonella, col. 6, lines 9-11 and 17-19). *It should be noted that the "continuity device/module" is analogous to the "short-circuit device."*

7. **As per claim 6**, the combination of Bonella/Arimilli/Chow discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module (Bonella, col. 6, lines 9-11 and 17-19).

8. Claims 2, 4, 5, 7, 8, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonella in view of Arimilli, Chow, and Lasker et al. (U.S. Patent 5,586,291).

9. **As per claim 2**, Bonella discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data (Fig. 3; col. 8, lines 41-46; Figs. 13A and 13B, elements 140A-140H and 142A-142H) and buffer sections for sending and receiving the data (col. 9, line 40 – col. 10, line 7; Fig. 15);

a CPU which controls said control device for access operation to said memory modules (col. 1, lines 23-28), *See the citation note for the same limitation in claim 1 above.*

wherein said buffer sections are connected in series to form a ring bus with said control device (col. 3, lines 48-50; Fig. 3);

Bonella does not disclose a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which, when an arbitrary memory module is being replaced, switches an operational mode of a ring bus from a unidirectional bus which either send or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally, detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested;

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Arimilli discloses a control device which, when an arbitrary memory module is being replaced, switches an operational mode of a ring bus from a unidirectional bus which either send or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally (paragraph 0016; paragraph 0019; paragraph 0005; paragraph 0014; Fig. 1; Fig. 2); *See the citation note for the same limitation in claim 1 above.*

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus (paragraph 0017; Fig. 2, element 22);

a second buffer circuit for sending a signal to one input/output end of the ring bus (paragraph 0017; Fig. 2, element 21);

a third buffer circuit for receiving a signal from the other input/output end of the ring bus (paragraph 0018; Fig. 2, element 24);

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus (paragraph 0018; Fig. 2, element 25);

Bonella and Arimilli are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Arimilli's mode selectable transmitter/receiver within Bonella's memory controller such that when an arbitrary memory module is being replaced, the memory controller switches an operational mode of a ring bus from a unidirectional bus which either send or receives a signal unidirectionally, to a bi-directional bus which sends and receives a signal bi-directionally because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of the increased flexibility provided by a memory module system that is selectable between a bidirectional mode and a unidirectional mode.

The combination of Bonella/Arimilli does not disclose a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to

the detected address space at the time when an access to said memory module being replaced is requested.

Chow discloses a hard disk device to which the data stored in said memory modules is copied at predetermined time periods (paragraphs 0135-0136; paragraph 154Fig. 14, elements 110, 130, and 425; paragraph 0154); *See the citation note for the same limitation in claim 1 above.*

The combination of Bonella/Arimilli and Chow are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chow's non-volatile storage module and management module within Bonella/Arimilli's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of a storage system that is scalable, fault-tolerant, and easily maintained.

The combination of Bonella/Arimilli/Chow does not disclose a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested.

Lasker discloses a storage to which data stored in an arbitrary memory module is temporarily copied (col. 9, lines 42-43; Fig. 2, elements 34a' and 34b'); *It should noted that "NVSIMM 34b'" is analogous to "memory module" and "NVSIMM 34a' " is analogous to "storage."*

a control device which detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested (col. 9, lines 38-48; col. 15, line 66 – col. 16, line 2; Fig. 2, elements 40, 34a', and 34b'; Fig. 6, element 122). *It should be noted that "cache memory control circuit" is analogous to "control device." It should be also be noted that when NVSIMM 34a' is placed into a different controller for the failed NVSIMM 34b' it is required cache memory control circuit detect an address space of NVSIMM 34b', copy data corresponding to the detected address space (i.e. the same data corresponding to the detected address space from said hard disk device) from NVSIMM 34b' to NVSIMM 34a', and then access a memory area in NVSIMM 34a' at the time when an access to NVSIMM 34b' is requested. Finally, it should be noted the "DMA transfer between the disk drives and the cache memory of the disk controller" is analogous to "copying data corresponding to the detected address space from said hard disk device to said storage."*

The combination of Bonella/Arimilli/Chow and Lasker are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lasker's mirror mode modules within Bonella/Arimilli/Chow's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the potential for data loss.

10. **As per claim 5**, Bonella discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data (Fig. 3; col. 8, lines 41-46; Figs. 13A and 13B, elements 140A-140H and 142A-142H) and buffer sections for sending and receiving the data (col. 9, line 40 – col. 10, line 7; Fig. 15);

a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module (col. 6, lines 9-11 and 17-19);

a CPU which controls said control device for access operation to said memory modules (col. 1, lines 23-28), *See the citation note for the same limitation in claim 1 above.*

Bonella does not disclose a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which, when an arbitrary memory module is being replaced, detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested;

wherein said buffer sections are connected in series to form a unidirectional bus which either sends or receives a signal unidirectionally,

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus;

a second buffer circuit for sending a signal to one input/output end of the ring bus;

a third buffer circuit for receiving a signal from the other input/output end of the ring bus;

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus.

Arimilli discloses wherein said buffer sections are connected in series to form a unidirectional bus which either sends or receives a signal unidirectionally (paragraph 0016; Fig. 2);

and wherein said control device comprises:

a first buffer circuit for receiving a signal from one input/output end of the ring bus (paragraph 0017; Fig. 2, element 22);

a second buffer circuit for sending a signal to one input/output end of the ring bus (paragraph 0017; Fig. 2, element 21);

a third buffer circuit for receiving a signal from the other input/output end of the ring bus (paragraph 0018; Fig. 2, element 24);

and a fourth buffer circuit for sending a signal to the other input/output end of the ring bus (paragraph 0018; Fig. 2, element 25);

Bonella and Arimilli are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Arimilli's mode selectable transmitter/receiver within Bonella's memory controller because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of the increased flexibility provided by a memory module system that is selectable between a bidirectional mode and a unidirectional mode.

The combination of Bonella/Arimilli does not disclose a hard disk device to which the data stored in said memory modules is copied at predetermined time periods;

a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested.

Chow discloses a hard disk device to which the data stored in said memory modules is copied at predetermined time periods (paragraphs 0135-0136; paragraph 154Fig. 14, elements 110, 130, and 425; paragraph 0154); *See the citation note for the same limitation in claim 1 above.*

The combination of Bonella/Arimilli and Chow are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chow's non-volatile storage module and management module within Bonella/Arimilli's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of a storage system that is scalable, fault-tolerant, and easily maintained.

The combination of Bonella/Arimilli/Chow does not disclose a storage to which data stored in an arbitrary memory module is temporarily copied;

a control device which detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk

device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested.

Lasker discloses a storage to which data stored in an arbitrary memory module is temporarily copied (col. 9, lines 42-43; Fig. 2, elements 34a' and 34b'); *See the citation note for the same limitation in claim 2 above.*

a control device which detects an address space of said memory module to be replaced, copies data corresponding to the detected address space from said hard disk device to said storage, and accesses a memory area in said storage corresponding to the detected address space at the time when an access to said memory module being replaced is requested (col. 9, lines 38-48; col. 15, line 66 – col. 16, line 2; Fig. 2, elements 40, 34a', and 34b'; Fig. 6, element 122). *See the citation note for the same limitation in claim 2 above.*

The combination of Bonella/Arimilli/Chow and Lasker are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lasker's mirror mode modules within Bonella/Arimilli/Chow's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing the potential for data loss.

11. **As per claim 4**, the combination of Bonella/Arimilli/Chow/Lasker discloses a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module (Bonella, col. 6, lines 9-11 and 17-19). *See the citation note for claim 3 above.*

12. **As per claims 7 and 8**, the combination of Bonella/Arimilli/Chow/Lasker discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module (Bonella, col. 6, lines 9-11 and 17-19).

13. **As per claims 15 and 16**, the combination of Bonella/Arimilli/Chow/Lasker discloses said storage is a memory module for mirroring which is provided with a memory area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that in order for any data to be written to and copied from the NVSIMM 34a' it is required the NVSIMM 34a' have a some sort of "buffer section."*

14. **As per claims 17 and 18**, the combination of Bonella/Arimilli/Chow/Lasker discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that this limitation is merely an intended use of the claimed invention. Since Lasker's NVSIMM 34a' is capable of performing the intended use (i.e. capable of being a graphics memory), it therefore meets the claim.*

15. **As per claims 19 and 20**, the combination of Bonella/Arimilli/Chow/Lasker discloses said storage is free memory areas of the other memory modules excluding

said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that NVSIMM 34b' is the failed memory module to be replaced and the mirrored data is stored on the free area of NVSIMM 34a' (i.e. another memory module which is not the memory module being replaced).*

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bonella, Arimilli, and Chow as applied to claim 3 above, and further in view of Emerson et al. (U.S. Patent 6,487,623) (hereinafter "Emerson").

17. **As per claim 9**, the combination of the combination of Bonella/Arimilli/Chow discloses all the limitations of claim 9 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *It should be noted "FET signal isolation buffer" is analogous to "FET switch."*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *It should be noted that "hot-plug controller" is analogous to "control device." It should be noted that the FET isolation buffer's "disconnect" mode is analogous to the "turning ON the FET switch" and conversely the FET isolation buffer's "connect" mode is analogous to "turning OFF the FET switch." The actual states of "ON" and "OFF" are arbitrary and solely dependent on whether a PMOS or NMOS is being used as the FET.*

The combination of Bonella/Arimilli/Chow and Emerson are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Emerson's FET isolation buffers and hot-plug controller within Bonella/Arimilli/Chow's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of transparent automatic memory fail-over.

18. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonella, Arimilli, Chow, and Lasker as applied to claims 4 and 5 above, and further in view of Emerson.

19. **As per claims 10 and 11**, the combination of the combination of Bonella/Arimilli/Chow/Lasker discloses all the limitations of claims 10 and 11 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *See the citation note for the same limitation in claim 9 above.*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *See the citation note for the same limitation in claim 9 above.*

The combination of Bonella/Arimilli/Chow/Lasker and Emerson are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Emerson's FET isolation buffers and hot-plug controller within Bonella/Arimilli/Chow/Lasker's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of transparent automatic memory fail-over.

20. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bonella, Arimilli, and Chow as applied to claim 3 above, and further in view of Perego et al. (U.S. Patent 6,889,304) (hereinafter "Perego").

21. **As per claim 12**, the combination of the combination of Bonella/Arimilli/Chow discloses all the limitations of claim 12 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Perego discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (col. 10, lines 14-21).

The combination of Bonella/Arimilli/Chow and Perego are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Perego's shorting connector within Bonella/Arimilli/Chow's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing additional flexibility to the system by shorting contacts when no memory module is inserted and then releasing the short when a memory module is inserted.

22. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonella, Arimilli, Chow, and Lasker as applied to claims 4 and 5 above, and further in view of Perego.

23. **As per claims 13 and 14**, the combination of the combination of Bonella/Arimilli/Chow/Lasker discloses all the limitations of claims 13 and 14 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Perego discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with shorting pins

which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (col. 10, lines 14-21).

The combination of Bonella/Arimilli/Chow/Lasker and Perego are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Perego's shorting connector within Bonella/Arimilli/Chow/Lasker's ring bus memory module system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing additional flexibility to the system by shorting contacts when no memory module is inserted and then releasing the short when a memory module is inserted.

Response to Arguments

24. With respect to Applicant's argument regarding Lasker's cache memory, on page 18 of the communication filed June 16, 2008, the Examiner respectfully disagrees. Applicant alleges that Lasker's cache memory is "transient" and therefore does not copy data stored in said memory modules. However, it matters not how long data stays in the cache memory before it is de-allocated, the fact of the matter is the data is stored in the cache memory for a finite period of time. Thus, Lasker's NVSIMM 34a' (cache memory) is a storage to which data stored on NVSIMM 34b' (an arbitrary memory

module) is temporarily stored (i.e. copied). Accordingly, Lasker sufficiently discloses a storage to which data stored in an arbitrary memory module is temporarily copied.

25. With respect to Applicant's argument regarding Emerson's FET isolation buffers, on page 22 of the communication filed June 16, 2008, the Examiner respectfully disagrees. Applicant appears to be again attacking Emerson individually because Emerson discloses a parallel bus structure. The rejection of claim 9 is not based on individual references, but rather the combination of Bonella, Arimilli, Chow, and Emerson. When combining Bonella, Arimilli, Chow, and Emerson, as set forth by the Examiner above, Emerson's FET isolation buffers are implemented within Bonella/Arimilli/Chow ring bus memory module system, which uses a ring bus architecture. As noted in the Office action dated February 15, 2008, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

26. All of Applicant's additional arguments filed June 16, 2008 with respect to **claims 1-20** have been considered but are moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-20** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
October 9, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185